10GBASE-LR SFP+ Optical Transceiver

Preliminary

FEATURES

- **RoHS compliant**
- **Compliant to SFP+ Electrical MSA SFF-8431**
- **Compliant with SFF-8472 MSA**
- **Standard LC duplex fiber-optic connector**
- **I^2C for integrated Digital Optical Monitoring**
- **Power consumption ＜1W**

Description

The LCP-10G3B4QDR is a hot pluggable 10Gbps small form factor plus transceiver module integrated with the high performance 1310nm DFB Laser transmitter, high sensitivity linear PD-TIA receiver for 10Gbps applications. It is compliant with the SFF-8431 SFP+ Electrical Multi-source Agreement (MSA) with five digital monitoring functions: Temperature, Vcc, Tx optical power, Tx laser bias current and Rx received optical power.

Applications

- 10G LAN switch
- 10G Ethernet switch/router
- 10G Fiber channel
- SAN applications

Performance

- LCP-10G3B4QDR: Link distance up to 10km over 9um SMF

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Storage Temperature	T_S	-40		85	ºC
Supply Voltage Range @3.3V	V_{CC3}	-0.5		3.6	V

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Case Operating Temperature	T_C	-5		+70	ºC
Supply Voltage @3.3V	V_{CC3}	3.135	3.30	3.465	V
Relative Humidity (non condensation)	-	5		85	%
DC Common Mode Voltage	V_{CM}	0		3.6	V

Low Speed Electrical Characteristics

(V_{CC}=3.135V to 3.465V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Total Supply Current	I_{CC}			300	mA	
Power Consumption	PC			1	W	
TX_Fault, RX_LOS	V_{OL}	0		0.4	V	
	V_{OH}	Host_Vcc-0.5		Host_Vcc+0.3	V	
TX_Disable	V_{IL}	-0.3		0.8	V	1
	V_{IH}	2.0		VccT+0.3	V	1
RS0, RS1	V_{IL}	-0.3		0.8	V	2
	V_{IH}	2.0		VccT+0.3	V	2

1. Shall be pulled up with 4.7k-10k ohms to 3.3 volt in the module.
2. Shall be pulled low to GND with a ＞30k ohms resistor in the module.

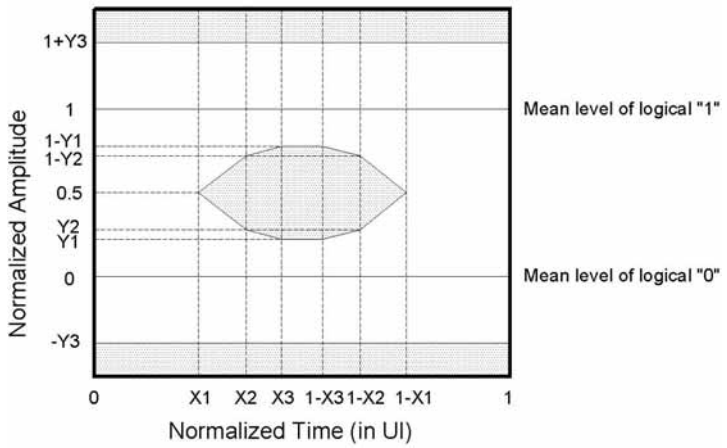
Optical Transmitter Characteristics (T_C = -5℃ to 70℃)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Signaling speed (nominal)	R		10.3125		Gb/s	
Signaling speed variation from nominal				±100	ppm	
Center Wavelength	λ	1260		1355	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Optical Modulaion Amplitude	OMA	-5.2			dBm	
Average output power	AP	-8.2		+0.5	dBm	
Extinction Ratio	ER	3.5			dB	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.40, 0.45, 0.25, 0.28, 0.40}				

Notes:

1. Even if the TDP < 1 dB, the OMA (min) must exceed this value.

Transmitter eye mask definition



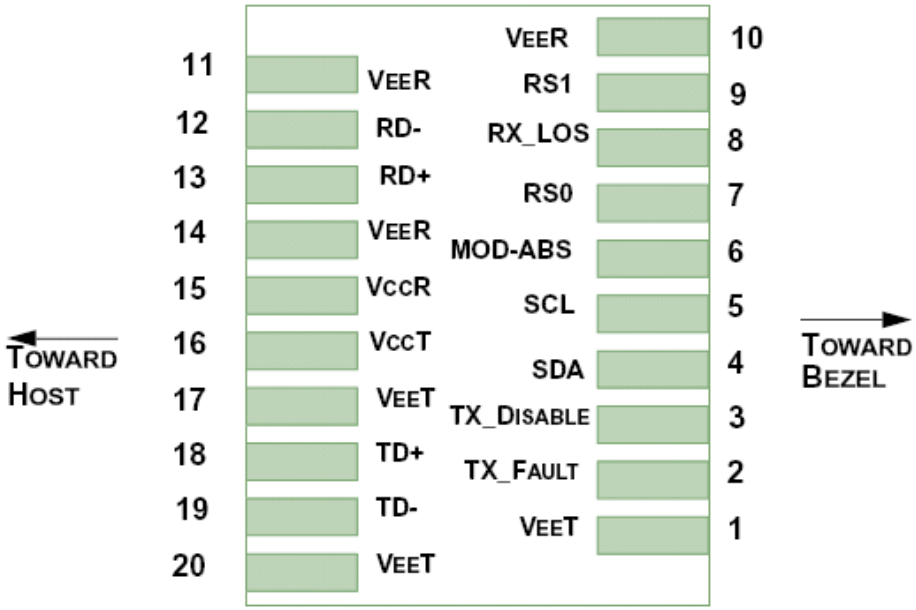
4. Optical Receive Characteristics (T_C=0 ºC to 70 ºC)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Signaling speed (nominal)	Ts		10.3125		Gb/s	
Signaling speed variation from nominal				±100	ppm	
Center Wavelength	λ	1260		1355	nm	
Overload	P_O			0.5	dBm	
Receiver sensitivity in OMA	RSO			-12.6	dBm	[1]
Stressed Receiver sensitivity in OMA	SRS			-10.3	dBm	[1]
LOS De-assert	LOS_D			-18	dBm	
LOS Assert	LOS_A	-30			dBm	

Notes:

1. Measured with 2^31-1 PRBS for BER = 10^{-12}. Per IEEE802.3ae

SFP+ Transceiver Electrical Pad Layout



Module Electrical Pin Definition

Pin	Logic	Symbol	Name/Description	Note
1		VeeT	Module Transmitter Ground	1
2	LVTTL-O	TX_Fault	Module Transmitter Fault	2
3	LVTTL-I	TX_Disable	Transmitter Disable; Turns off transmitter laser output	3
4	LVTTL-I/O	SDA	2- write Serial Interface Data Line	
5	LVTTL-I/O	SCL	2- write Serial Interface Clock	
6		MOD_ABS	Module Absent, connected to $V_{ee}T$ or $V_{ee}R$ in the module	4
7	LVTTL-I	RS0	Not Implement	
8	LVTTL-O	RX_LOS	Receiver Loss of Signal Indication	2
9	LVTTL-I	RS1	Not Implement	
10		VeeR	Module Receiver Ground	1
11		VeeR	Module Receiver Ground	1
12	CML-O	RD-	Receiver Inverted Data Output	
13	CML-O	RD+	Receiver Non-Inverter Data Output	
14		VeeR	Module Receiver Ground	1
15		VccR	Module Receiver 3.3V Supply	
16		VccT	Module Transmitter 3.3V Supply	
17		VeeT	Module Transmitter Ground	1
18	CML-I	TD+	Transmitter Non-Inverted Data Input	
19	CML-I	TD-	Transmitter Inverted Data Input	
20		VeeT	Module Transmitter Griund	1

Note:

1. The module signal ground pins, VeeR and VeeT, shall be isolated from the module case.
2. This pin is an open collector/drain output pin and shall be pulled up with 4.7k-10k ohms to Host_Vcc on the host board. Pull ups can be connected to multiple power supplies, however the host board design shall ensure that no module pin has voltage exceeding module VccT/R + 0.5V.
3. This pin is an open collector/drain input pin and shall be pulled up with 4.7k-10k ohms to VccT in the Module.
4. This pin shall be pulled up with 4.7k-10k ohms to Host_Vcc on the host board.

Low speed electrical control pins and 2-wire interface

In addition to the 2-wire serial interface, the SFP+ module has the following low speed pins for control and status:

- TX_Fault
- TX_Disable
- RS0/RS1
- MOD_ABS
- RX_LOS

1 TX_Fault

.TX_Fault is a module output pin that when High, indicates that the module transmitter has detected a fault condition related to laser operation or safety.
The TX_Fault output pin is an open drain/collector and must be pulled p to the Host_Vcc with 4.7k-10k ohms on the host board

2 TX_Disable

TX_Disable is a module input pin. When TX_Disable is asserted High or Left open, the SFP+ module transmitter output must be turned off. The TX_DIS pin must be pulled up to VccT in the SFP+ module..

3 RS0/RS1

RS0 and RS1 are module input rate select pins and are pulled low to VeeT with a > 30kΩ resistor in the module. RS0 is an input hardware pin which optionally selects the optical receive data path rate coverage for an SFP+ module. RS1 is an input hardware pin which optionally selects the optical transmit path data rate coverage for an SFP+ module.

4 MOD_ABS

Mod_ABS is pulled up to Host_Vcc with 4.7k-10k ohms on the host board and connected to VeeT or VeeR in the SFP+ module. MOD_ABS is then asserted “High” when the SFP+ module is physically absent from a host slot. In the SFP MSA (INF8074i) this pin had the same function but is called MOD_DEF0.

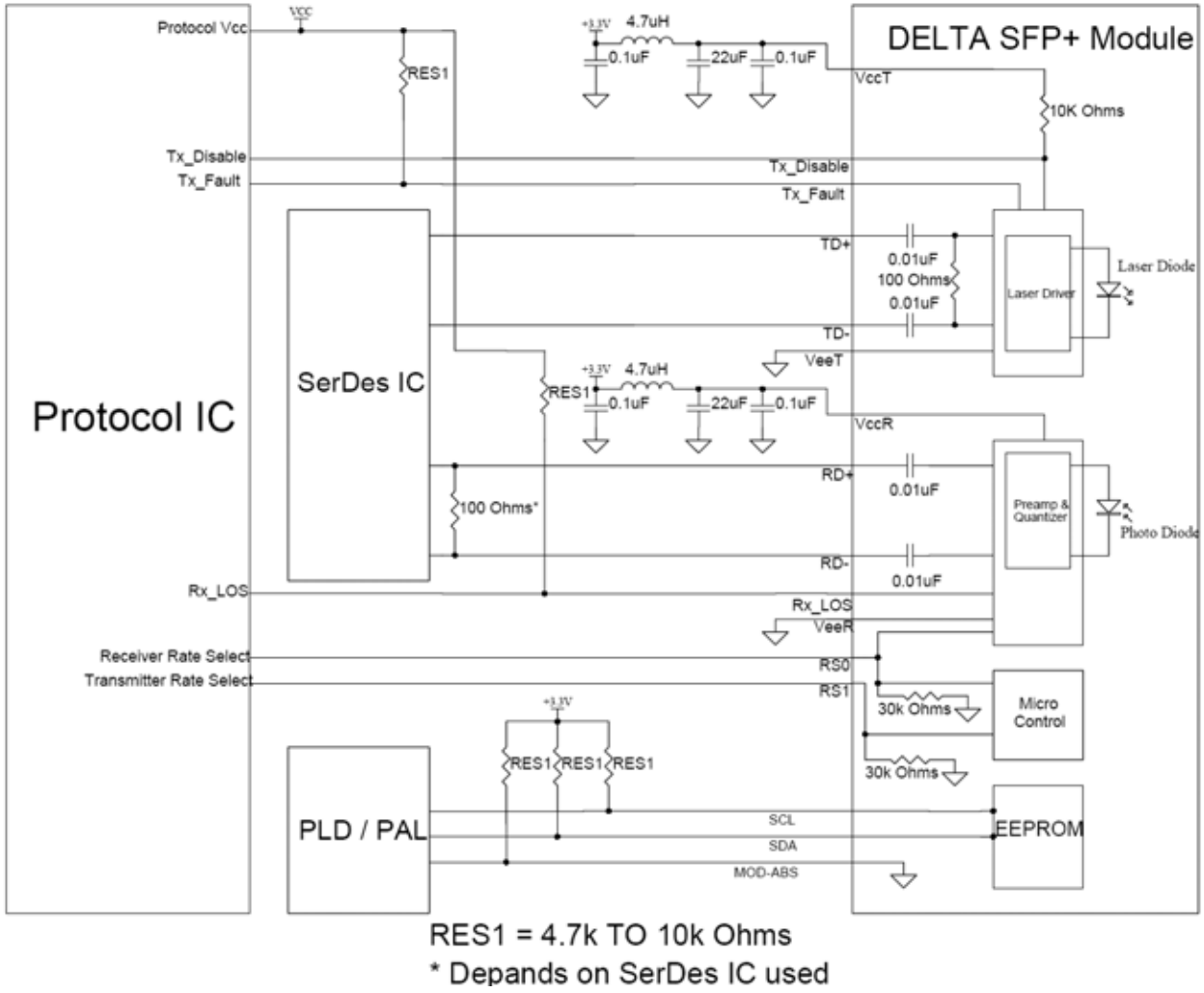
5 SCL/SDA

SCL is the 2-wire interface clock and SDA is the 2-wire interface data line. SCL and SDA are pulled up to a voltage in the range of 3.14V to 3.46V on the host.

6 RX_LOS

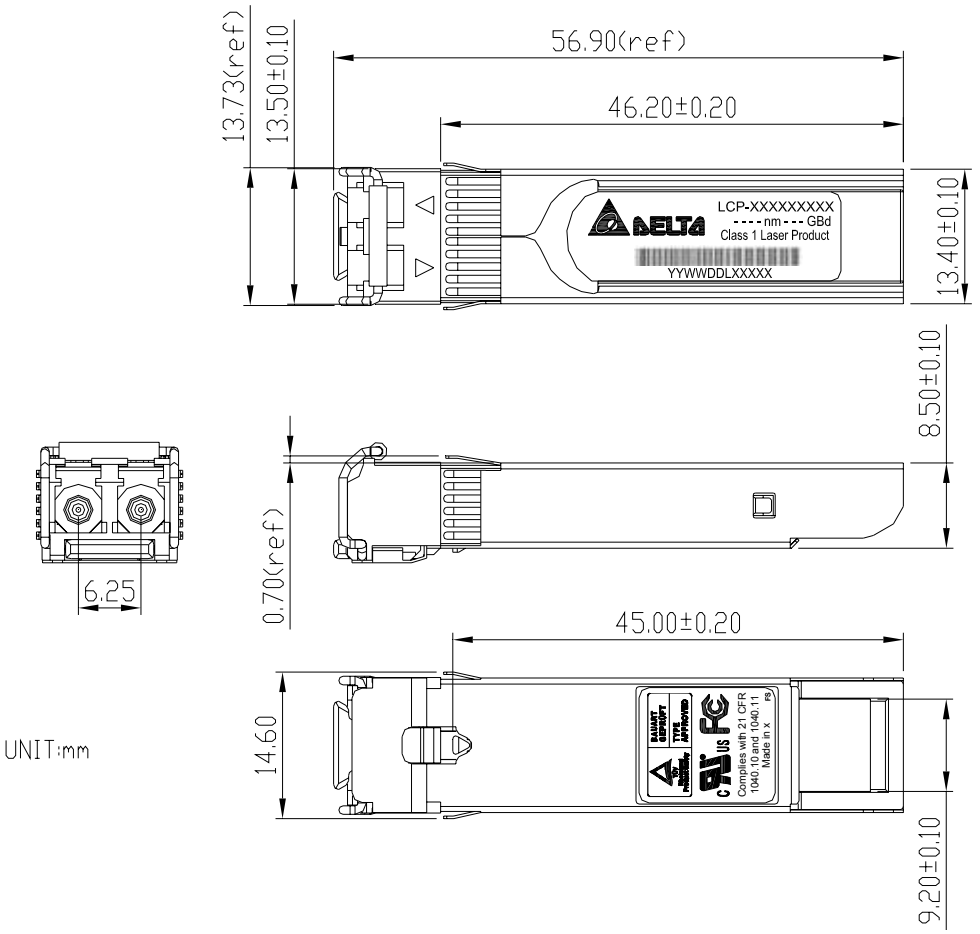
RX_LOS when High indicated an optical signal level below that specified in the relevant standard. The RX_LOS pin is an open drain/collector output and must be pulled up to host Vcc with a 4.7k-10k ohms on the host board.
RX_LOS assert min and de-assert max are defined in the relevant standard. To avoid spurious transition of RX_LOS a minimum hysteresis of 0.5 dB is recommended.

Recommend Circuit Schematic



Package Outline Drawing for Metal Housing with Bail de-latch

Latch Color Identifier
Blue



Timing parameters for SFP+ management

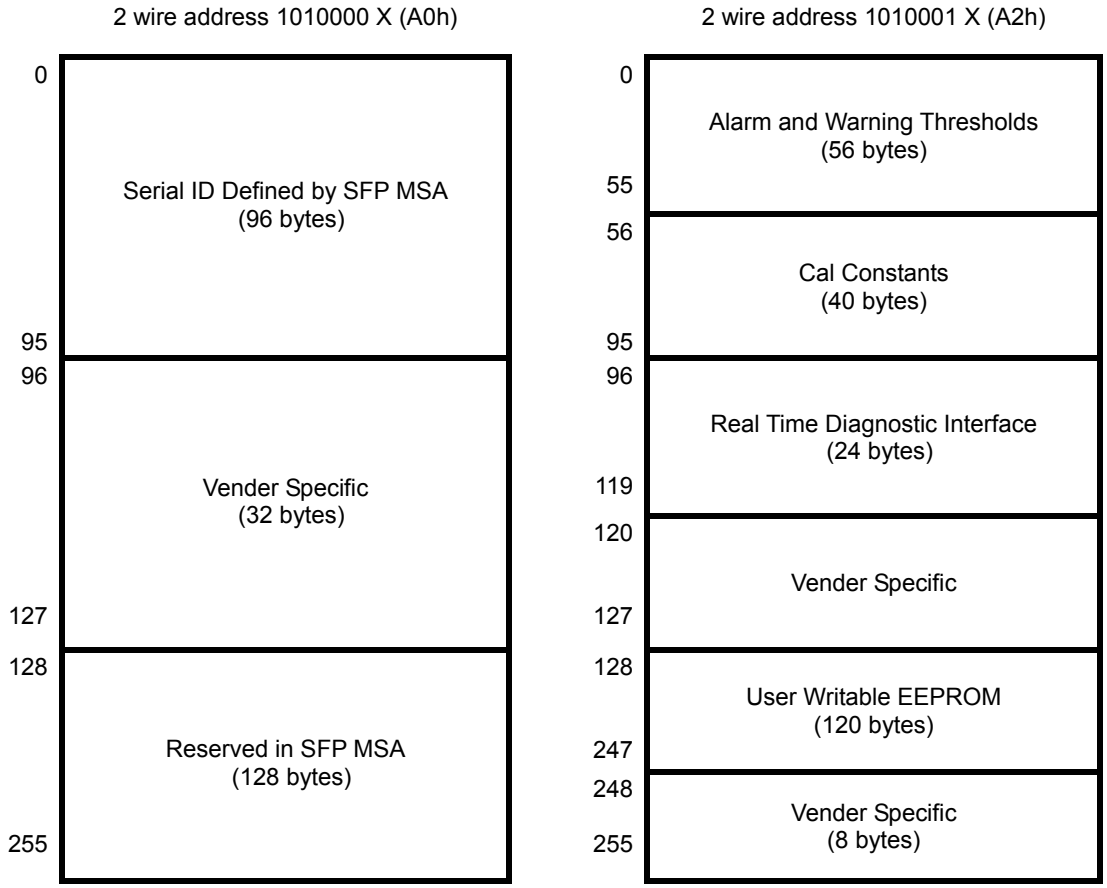
Parameter	Symbol	Min.	Max.	Unit	Note
TX_DISABLE Assert time	t_off		10	μsec	1
TX_DISABLE Negate time	t_on		2	msec	2
Time to initialize 2-wire interfase	t_2w_start_up		300	msec	3
Time to initialize	t_start_up		300	msec	4
Time to initialize cooled module	t_start_up_cooled		90	sec	4
Time to Power Up to Level 2	t_power_level2		300	msec	5
Time to Power Down from Level 2	T_power_down		300	msec	6
TX_Fault assert	TX_Fault_on		1	msec	7
TX_Fault assert for cooled module	TX_Fault_on		50	msec	7
TX_Fault Reset	t_reset	10		μsec	8
Module Reset	t_module_reset		TBD	msec	TBD
RS0, RS1 rate select timing for FC	t_RS0_FC, RS1_FC		500	μsec	9
RS0, RS1 rate select timing non FC	t_RS0, t_RS1		10	msec	9
RX_LOS assert delay	t_los_on		100	μsec	10
RX_LOS negate delay	t_los_off		100	μsec	11

Notes:

1) Rising edge of TX_Disable to fall of output signal below 10% of nominal.
2) Falling edge of TX_Disable to rise of output signal above 90% of nominal. This only applies in normal operation, not during start up or fault recovery.
3) From power on or negation of TX_Disable.
4) From power on or TX_Disable negated during power up, or TX_Fault recovery, until non-cooled power level 1 part (or non-cooled power level 2 part already enabled at power level 2 for TX_Fault recovery) is fully operational.
5) From falling edge of stop bit enabling power level 2 until non-cooled module is fully operational.
6) From falling edge of stop bit disabling power level 2 until module is within power level 1 requirements.
7) From Occurrence of fault to assertion of TX_Fault.
8) Time TX_Disable must be held High to reset TX_Fault.
9) From assertion till stable output.
10) From Occurrence of loss of signal to assertion of LOS
11) From Occurrence of presence of signal to negation of RX_LOS.

Enhanced Digital Diagnostic Interface

The memory map in the following describes an extension to the memory map defined in SFP MSA. The enhanced interface uses the two wire serial bus address 1010001X(A2h) to provide diagnostic information about the module's present operating conditions.



Digital Diagnostic Memory Map Specific Data Field Descriptions

EEPROM Serial ID Memory Contents (2-Wire Address A0h)

Address	Hex	ASCII	Address	Hex	ASCII	Address	Hex	ASCII
00	03		43	2D	-	86	DC	
01	04		44	31	1	87	DC	
02	07		45	30	0	88	DC	
03	20	10G Base-LR	46	47	G	89	DC	
04	00		47	33	3	90	DC	
05	00		48	42	B	91	DC	
06	00		49	34	4	92	68	
07	00		50	51	Q	93	F0	
08	00		51	44	D	94	03	
09	00		52	52	R	95	CS2	Note 4
10	00		53	20		96	00	
11	03		54	20		97	00	
12	67		55	20		98	00	
13	00		56	41		99	00	
14	0A	10km	57	20		100	00	
15	64	10km	58	20		101	00	
16	00		59	20		102	00	
17	00		60	05	1310nm	103	00	
18	00		61	1E	1310nm	104	00	
19	00		62	00		105	00	
20	44	D	63	CS1	Note 1	106	00	
21	45	E	64	01		107	00	
22	4C	L	65	1A		108	00	
23	54	T	66	00		109	00	
24	41	A	67	00		110	00	
25	20		68	SN	Note 2	111	00	
26	20		69	SN		112	00	
27	20		70	SN		113	00	
28	20		71	SN		114	00	
29	20		72	SN		115	00	
30	20		73	SN		116	00	
31	20		74	SN		117	00	
32	20		75	SN		118	00	
33	20		76	SN		119	00	
34	20		77	SN		120	00	
35	20		78	SN		121	00	
36	00		79	SN		122	00	
37	00		80	SN		123	00	
38	00		81	SN		124	00	
39	00		82	SN		125	00	
40	4C	L	83	SN		126	00	
41	43	C	84	DC	Note 3	127	00	
42	50	P	85	DC		128	00	Note 5

Notes:

1) Byte 63: Check sum of bytes 0-62.
2) Byte 68-83: Serial number.
3) Byte 84-91: Date code.
4) Byte 95: Check sum of bytes 64-94.
5) Byte 128 to 255 had been set hex 00.

Digital Diagnostic Monitoring Interface

Alarm and Warning Thresholds (2-Wire Address A2h)

Address	# Bytes	Name	Value (Dec.)	Unit	Note
00-01	2	Temp High Alarm	T_C (MAX.)+8	℃	1
02-03	2	Temp Low Alarm	T_C (MIN.)-8		
04-05	2	Temp High Warning	T_C (MAX.)+3		
06-07	2	Temp Low Warning	T_C (MIN.)-3		
08-09	2	Voltage High Alarm	3.8	Volt	
10-11	2	Voltage Low Alarm	2.8		
12-13	2	Voltage High Warning	3.5		
14-15	2	Voltage Low Warning	3.1		
16-17	2	Bias High Alarm	I_{OP}*2+35	mA	2
18-19	2	Bias Low Alarm	I_{OP}-13		
20-21	2	Bias High Warning	I_{OP} *2+30		
22-23	2	Bias Low Warning	I_{OP} –8		
24-25	2	TX Power High Alarm	P_h+2	dBm	3
26-27	2	TX Power Low Alarm	P_l -2		
28-29	2	TX Power High Warning	P_h+1		
30-31	2	TX Power Low Warning	P_l -1		
32-33	2	RX Power High Alarm	P_0+2	dBm	4
34-35	2	RX Power Low Alarm	P_S-2		
36-37	2	RX Power High Warning	P_0+1		
38-39	2	RX Power Low Warning	P_S-1		
40-45	16	Reversed			
56-91	36	External Calibration Constants			
92-94	3	Reversed			
95	1	Checksum			5
96-97	2	Real Time Temperature			
98-99	2	Real Time Supply Voltage			
100-101	2	Real Time Tx Bias Current			
102-103	2	Real Time Tx Optical Power			
104-105	2	Real Time Rx Received Power			
106-109	4	Reserved			
110	1	Optional Status/ Control Bits			
111	1	Reserved			
112-119	8	Optional Set of Alarm and Warning			

Notes:

1) T_C: Case Operating temperature
2) I_{OP}: Operating current at room temperature. The min. setting current is 0 mA.
3) P_h: Maximum value of transmitter optical power
   P_l : Minimum value of transmitter optical power
4) P_0: Overload optical power of receiver
   P_S: Sensitivity optical power of receiver
5) Byte 95 contains the low order 8bits of sum of bytes 0~94

6)

State/ Control Bits

Byte	Bit	Name	Description
110	7	Tx Disable State	Digital state of the Tx disable input pin
110	6	Soft Tx Disable	Read/ Write bit that allow software disable of laser
110	5	Reserved	
110	4	Rate Select State	Rate Select State
110	3	Soft Rate Select	Software Rate Select State
110	2	Tx Fault	Digital state of the Tx fault output pin
110	1	LOS	Digital state of the LOS output pin.
110	0	Data_Ready_Bar	NA

7)

Optional Set of Alarm and Warning

Byte	Bit	Name	Description
112	7	Temp High Alarm	Set when internal temperature exceeds high alarm level
112	6	Temp Low Alarm	Set when internal temperature is below low alarm level
112	5	Vcc High Alarm	Set when internal supply voltage exceeds high alarm level
112	4	Vcc Low Alarm	Set when internal supply voltage is below low alarm level
112	3	Tx Bias High Alarm	Set when Tx Bias current exceeds high alarm level
112	2	Tx Bias Low Alarm	Set when Tx Bias current is below low alarm level
112	1	Tx Power High Alarm	Set when Tx output power exceeds high alarm level
112	0	Tx Power Low Alarm	Set when Tx output power is below low alarm level
113	7	Rx Power High Alarm	Set when received power exceeds high alarm level
113	6	Rx Power Low Alarm	Set when received power is below low alarm level
113	5-0	Reserved	
116	7	Temp High Warning	Set when internal temperature exceeds high warning level
116	6	Temp Low Warning	Set when internal temperature is below low warning level
116	5	Vcc High Warning	Set when internal supply voltage exceeds high warning level
116	4	Vcc Low Warning	Set when internal supply voltage is below low warning level
116	3	Tx Bias High Warning	Set when Tx Bias current exceeds high warning level
116	2	Tx Bias Low Warning	Set when Tx Bias current is below low warning level
116	1	Tx Power High Warning	Set when Tx output power exceeds high warning level
116	0	Tx Power Low Warning	Set when Tx output power is below low warning level
117	7	Rx Power High Warning	Set when received power exceeds high warning level
117	6	Rx Power Low Warning	Set when received power is below low warning level
117	5-0	Reserved	

Digital Diagnostic Monitor Accuracy

Parameter	Typical Value	Note
Transceiver Temperature	± 3℃	1
Power Supply Voltage	± 3%	2
TX Bias Current	± 10%	
TX Optical Power	± 1.5dB	
RX Optical Power	± 3dB	

Notes:

1) Temperature is measured internal to the transceiver

2) Voltage is measured internal to the transceiver

Regulatory Compliance

Feature	Test Method	Reference	Performance
Electromagnetic Interference (EMI)		FCC Part15 Class B EN 55022 Class B (CISPR 22A)	(1) Satisfied with electrical characteristics of product spec. (2) No physical damage
Radio Frequency Electromagnetic Field Immunity		IEC/EN 61000-4-3	
Electrostatic Discharge (ESD) to the Duplex LC Receptacle	Contact Discharge	IEC/EN 61000-4-2	
	Air Discharge	IEC/EN 61000-4-2	
Electrostatic Discharge (ESD) to the Electrical Pins	Human Body Model (HBM)	MIL-STD-883E Method 3015.7 EIA-JESD22-A114	
	Machine Model (MM)	EIA-JESD22-A115	
Laser Eye Safety	FDA/CDRH TUV	US FDA CDRH AEL Class 1 IEC/EN 60825-1 IEC/EN 60825-2	
Component Recognition	TUV UL/CSA	IEC/EN 60950-1 UL60950	